X-Band Monolithic Series Feedback LNA

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Abstract — **An X-band monolithic three-stage low-noise amplifier (LNA) employing series feedback has demonstrated 1.8-dB noise figure with 30.0-dB gain and an input VSWR less than 1.2:1 at 10 GHz. The key to this design is using monolithic technology to obtain an exactly repeatable series feedback inductance to achieve a simultaneous noise match and input VSWR match.**

I. Introduction

IN CONVENTIONAL LNA's, the common-source FET input stage is presented with an optimum noise match (Z_{opt}) to achieve minimum noise figure at the expense of exhibiting high input VSWR. However, to achieve optimum noise figure and low-input VSWR simultaneously for a single-ended amplifier, series feedback provides the solution. This is the first reported demonstration of the use of series feedback in a monolithic microwave integrated circuit (MMIC) to achieve state-of-the-art X-band performance.

II. History

Strutt and Van Der Ziel in their 1942 article, "Suppression of spontaneous fluctuations in amplifiers and receivers for electrical communication and measuring devices," reported that a feedback inductor inserted into the cathode lead of a common-cathode high-vacuum triode circuit might enhance the signal-to-noise ratio at high frequencies [1].

In 1974, Jakob Engberg presented equations as well as optimization procedures for the design of two-port low-noise amplifiers [2]. Engberg describes how a combination of shunt and series feedback and proper output loading can be used to achieve $Z_{opt} = S_{11}^*$. As only lossless feedback elements are used, Engberg states that the minimum noise measure M_{min} remains constant. He reports that this theory has been verified at UHF frequencies using hybrid circuits. Other researchers [3]–[5] have demonstrated hybrid amplifiers that employ reactive feedback for improved performance.

Monolithic technology provides the key in obtaining an exactly repeatable series feedback inductance. A high-impedance microstrip transmission line can be accurately modeled and reproduced in large quantity. Optimization of bond wire lengths to achieve the correct feedback impedance, as in a hybrid amp, is eliminated.

Manuscript received May 1, 1985; revised July 1, 1985. This work was supported in part by Air Force Wright Aeronautical Laboratories/Avionics Laboratory under Contract F33615-82-C-1766.

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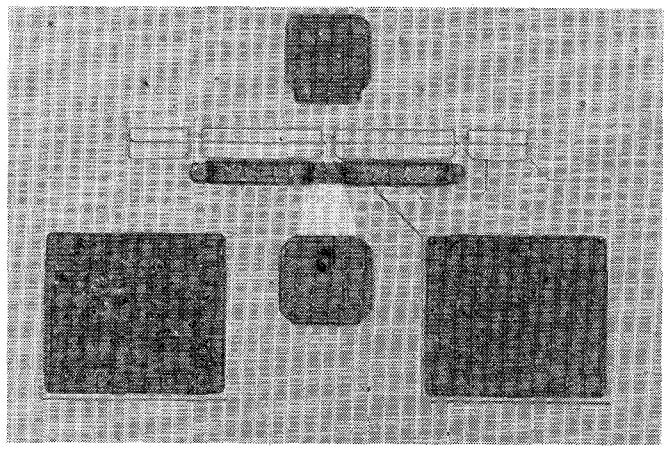

Fig. 1. "Monolithic-discrete" FET.

TABLE I
NOISE FIGURE AND GAIN DATA FOR "MONOLITHIC-DISCRETE" FET'S AT 10 GHz

TOTAL NUMBER FETs TESTED	NFmin (dB)			Associated Gain (dB)		
	LO	HI	AVG.	LO	HI	AVG.
75	1.5	1.9	1.7	9.5	11.5	11.0

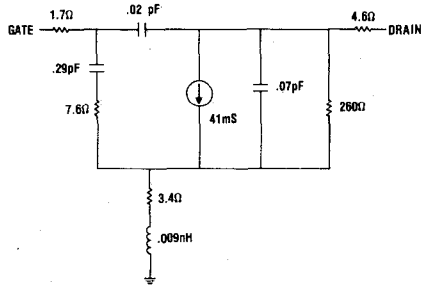

Fig. 2. "Monolithic-discrete" device model.

III. Device Characterization

A 0.5-μm gate length, 300-μm gate width FET, shown in Fig. 1, is used in each of the three stages. The active layer is formed by ion implantation. The device incorporates reactively ion-etched vias through 0.15-mm-thick GaAs to provide source grounding. Gate and drain terminals are brought to single bond pads to facilitate implementation into a monolithic circuit. The "monolithic-discrete" device is processed identically to the final MMIC, including deposition of the correct silicon nitride thickness to be used for the metal–insulator–metal (MIM) capacitors. This en-

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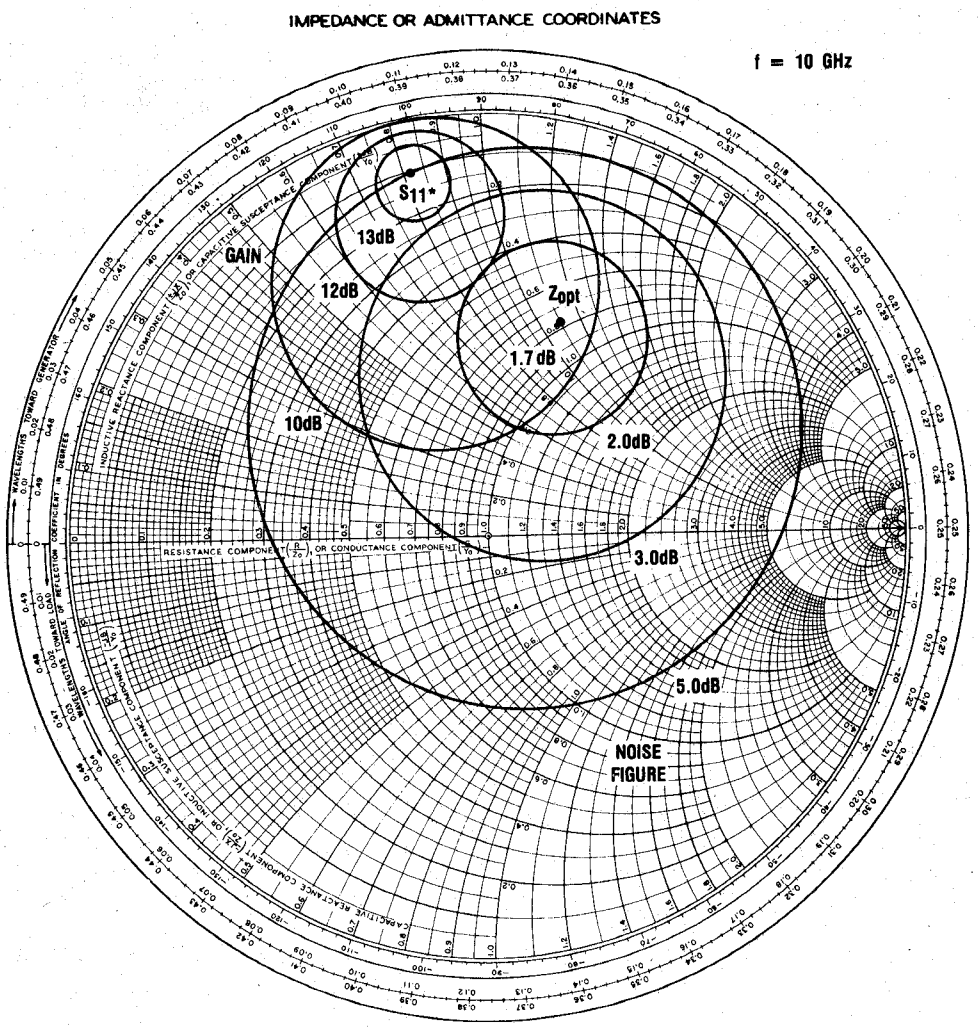

Fig. 3. 300-μm device noise figure and gain circles at 10 GHz.

sures that any change or increase in gate-drain and gate-source capacitances resulting from the increased capacitor dielectric thickness, which is greater than the standard discrete FET passivation thickness, is accounted for in the device characterization. The discrete FET is also fabricated on the same thickness GaAs as the MMIC so that the inductance of the vias can be properly modeled.

Several slices of these "monolithic-discrete" devices were evaluated for minimum noise figure (NF) and associated gain at 10 GHz. Table I shows a summary of the measured results from the 75 FET's tested. The minimum NF and associated gain are listed for both the best and worst FET measured, as well as the numerical average of all 75 FET's.

As the noise figure data indicates, the 75 monolithic discrete devices tested from four different slices exhibit similar RF performance. To examine the differences that exist from device to device, 16 FET's were selected for modeling. The equivalent circuit shown in Fig. 2 represents an average value model of the 16 FET's.

To aid in LNA designs and to better understand the device performance tradeoffs, the NF and gain circles of a typical device are plotted in Fig. 3. This device has a 1.7-dB minimum NF with 10.6 dB of associated gain at Z_{opt}. It is observed from Fig. 3 that a simultaneous conjugate match would result in a 5-dB NF. On the other hand, an optimum noise match would cause a 2.5-dB mismatch loss at the input, resulting in a 5:1 input VSWR.

IV. Circuit Design

Implementation of series feedback provides several advantages for low-noise amplifier design. Inductive reactance in the source lead of a common-source FET increases the real part of the input impedance. With proper impedance loading at the output of the FET, the conjugate of the FET input impedance and the optimum noise match impedance become coincident.

Impedance mapping on a Smith Chart is a useful design tool. Figs. 4 and 5 show the impedance maps of S_{11}^* and Z_{opt} as a function of inductive series feedback and output loading. In both plots, the inductive series feedback is incremented from 0.01 pH to 0.4 nH in 0.1 nH steps. In Fig. 4, the real part of the output load is varied from 25 to 50 to 100 Ω. In Fig. 5, the real part of the output load is fixed at 50 Ω and the imaginary part of the output load is

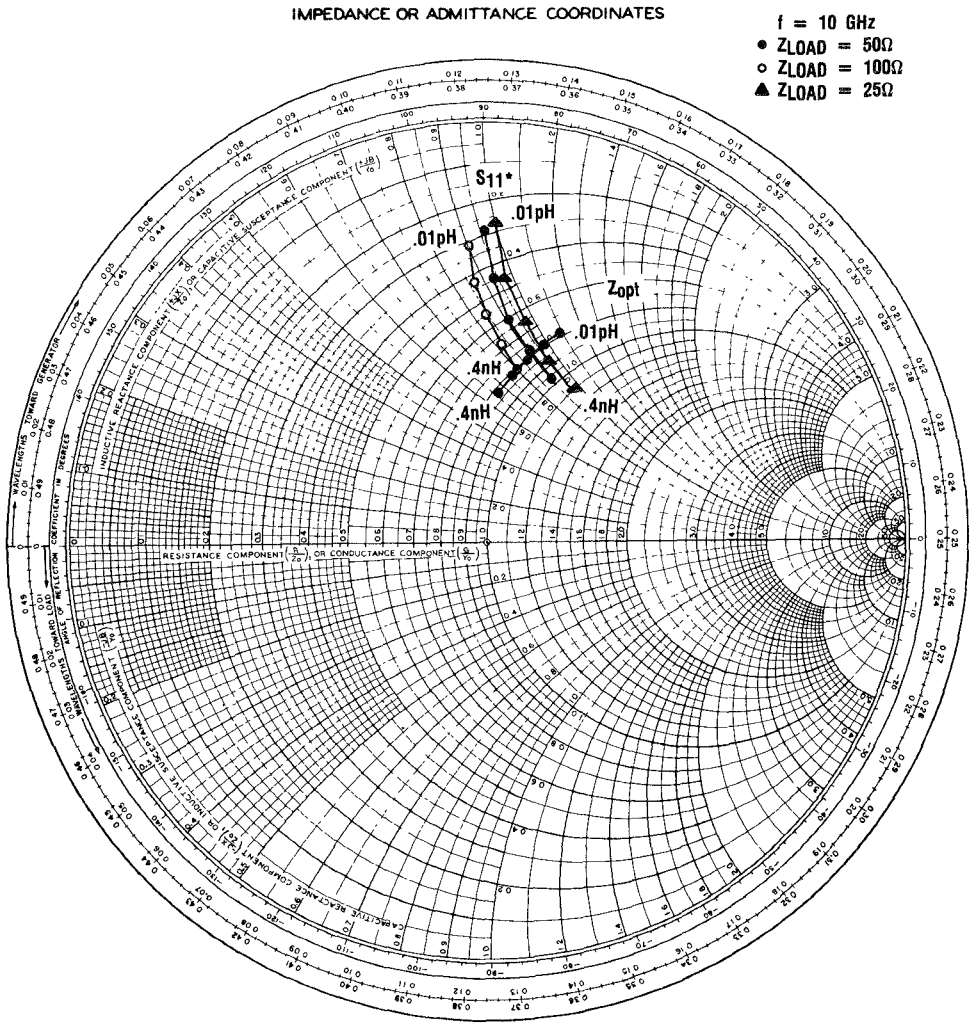

Fig. 4. Impedance mapping of S_{11}^* and Z_{opt} versus real part of output load and series feedback at 10 GHz.

varied $\pm 50\ \Omega$. It is observed that S_{11}^* of an FET is altered by both the feedback and the output loading, whereas Z_{opt} is unaffected by the output load and only varies with feedback. Using mapping techniques, it is possible to find a combination of inductive series feedback and output loading that results in S_{11}^* being equal to Z_{opt} at 10 GHz. Fig. 6 shows the NF circles and S_{11}^* for 0.28 nH of series feedback and an output load of 50-j25 Ω. Examination of Fig. 6 reveals several distinct advantages of using inductive series feedback, rather than another form of feedback (i.e., shunt or series resistive feedback). First, it is apparent that a simultaneous noise and gain match can be obtained with a proper choice of inductive feedback and output load. The other advantages become apparent when Fig. 6 is compared with Fig. 3. The minimum NF at Z_{opt} decreases from 1.7 to 1.6 dB. This reduction in NF_{min} with increasing feedback is consistent with the reduction in gain due to the addition of feedback. Lossless inductive feedback adds no noise to the circuit and therefore the minimum noise measure (M_{min}) of the device plus lossless feedback should remain constant [2]. Minimum noise measure is computed as

$$M_{min} = \frac{F_{min} - 1}{1 - \frac{1}{G_{av}}}$$

where G_{av} is the available gain of the FET with the input noise matched. For the example above, a sample calculation of M_{min} is shown in Table II. This drop in NF_{min} with a constant M_{min} has been experimentally verified with discrete FET's at 10 GHz.

Inductive series feedback decreases the equivalent noise resistance (r_n) of the two-port (device plus feedback). Series feedback also decreases the sensitivity to changes in the intrinsic device properties giving the final circuit greater tolerance to process variations. Inductive series feedback requires no dc blocking capacitor as in the case of shunt feedback. The feedback inductor (high-impedance line) can be realized monolithically in a very repeatable, high-yield

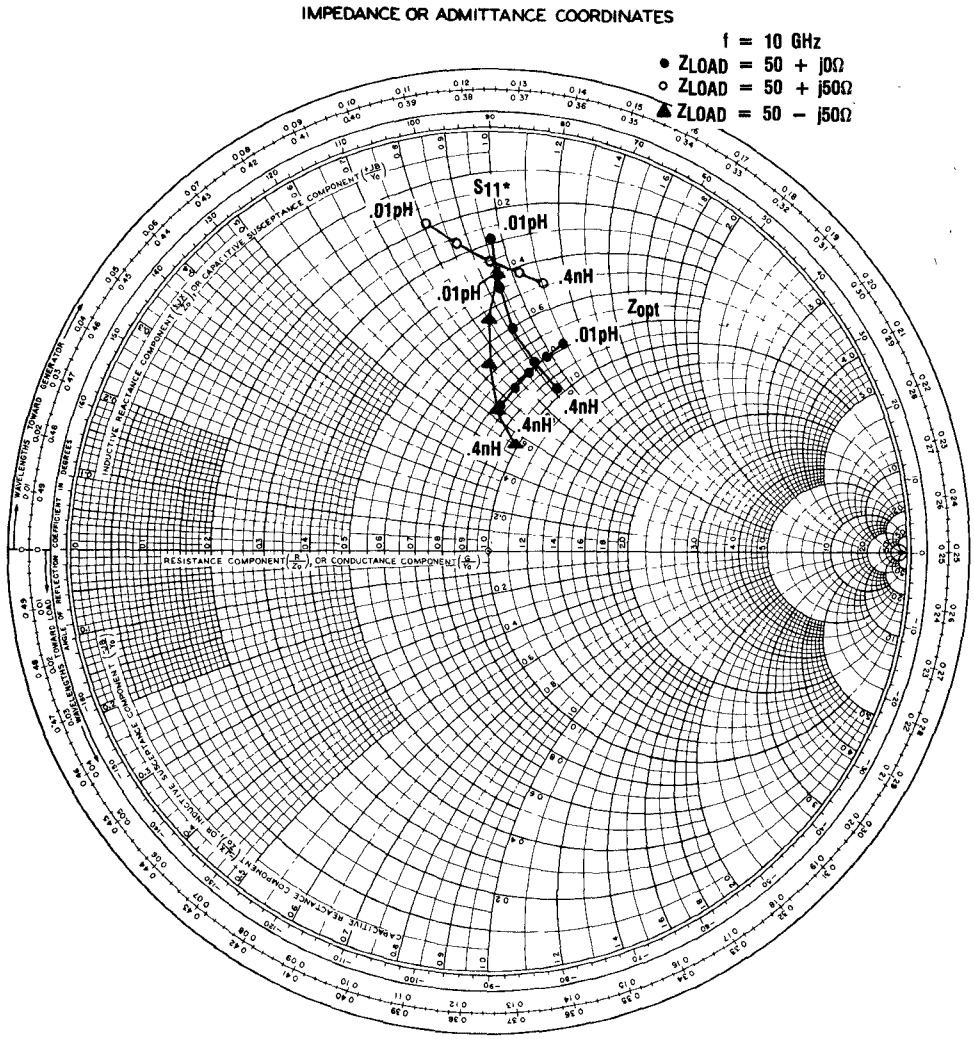

Fig. 5. Impedance mapping of S_{11}^* and Z_{opt} versus imaginary part of output load and series feedback at 10 GHz.

manner. The monolithic feedback element is fabricated on the semi-insulating GaAs substrate at the same process step as the RF transmission lines and the bottom plates of the MIM capacitors. No additional process steps or increased complexity are required.

The three-stage LNA circuit design is shown in Fig. 7. All RF matching and dc bias circuitry is included on the monolithic chip, shown in Fig. 8. The chip size is $3.0 \times 2.3 \times 0.15$ mm. Via holes are etched through the substrate and plated with gold to form low-resistance, low-inductance ground connections for the sources of the FET and the RF bypass capacitors. The gate and drain bias voltages are brought to common points at opposite corners of the chip. Gold–germanium–nickel–gold resistors are employed in the gate bias line to improve low-frequency stability.

V. RF Performance

The monolithic three-stage LNA with series feedback has demonstrated a 1.8-dB noise figure with 30.0-dB gain and an input VSWR less than 1.2:1 at 10 GHz. The X-band gain and noise figure response is shown in Fig. 9. Maximum noise figure is 2.0 dB from 8.5 to 11.5 GHz. From 9.0 to 11 GHz, input VSWR is less than 1.8:1. The input and output VSWR response is illustrated in Fig. 10. The amplifier, which is unconditionally stable, is operated at a drain bias of 3 V and a total drain current of 30 mA. Output power at 1-dB gain compression is 10 dBm.

Thirty-five LNA's from nine different slices have been evaluated for NF, gain, and VSWR. TAble III shows a summary of the results obtained from each slice at 10 GHz. LNA's were evaluated at bias conditions for minimum NF. The best and worst LNA measured as well as the average of all LNA's from that slice are recorded.

VI. Conclusions

An X-band monolithic three-stage LNA using series feedback has demonstrated excellent gain, noise figure, and input VSWR performance. Results from thirty-five LNA's

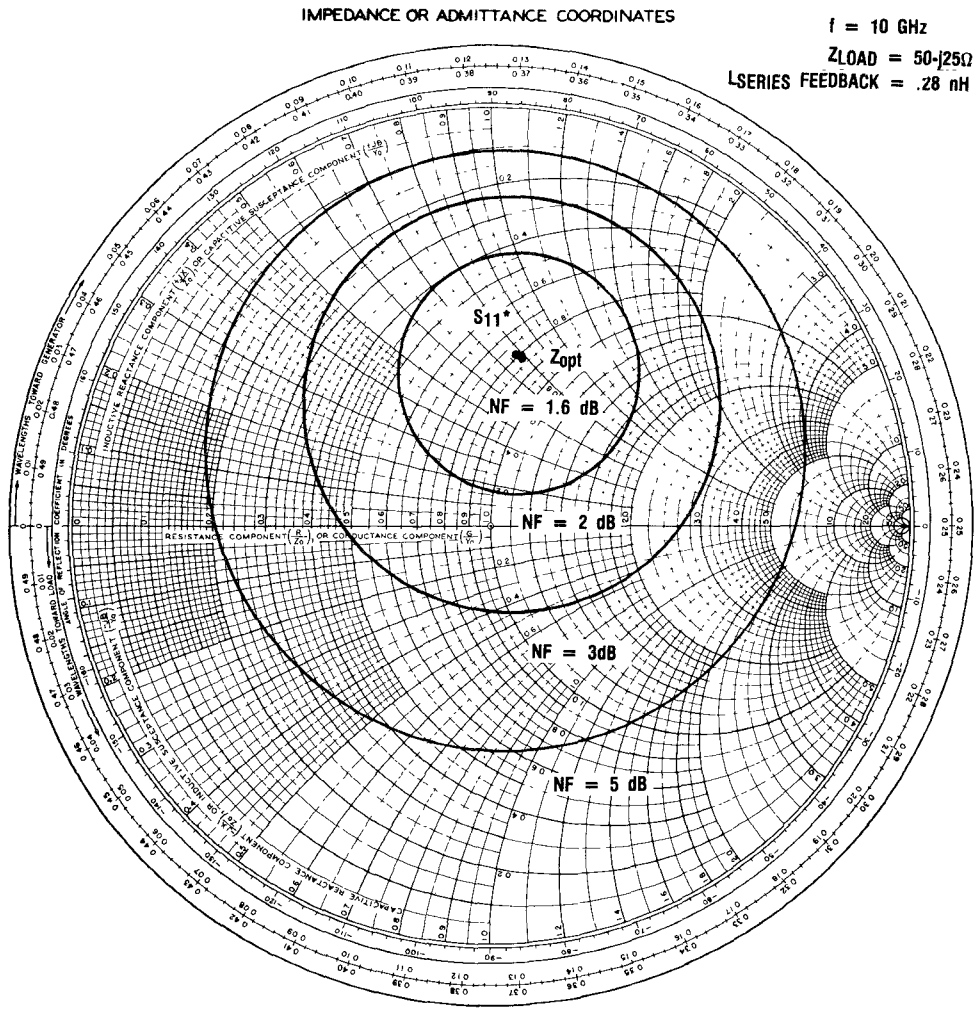

Fig. 6. NF circles and S_{11}^* for 0.28 nH of series feedback at 10 GHz.

TABLE II
CALCULATION OF MINIMUM NOISE MEASURE AT 10 GHZ

SERIES FEEDBACK INDUCTANCE	NFmin (dB)	Gain (dB)	Mmin
01pH	1 7	10 6	52
28nH	1 6	8 4	52

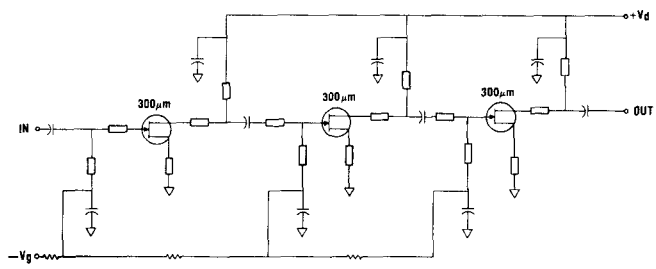

Fig. 7. Monolithic three-stage LNA circuit schematic.

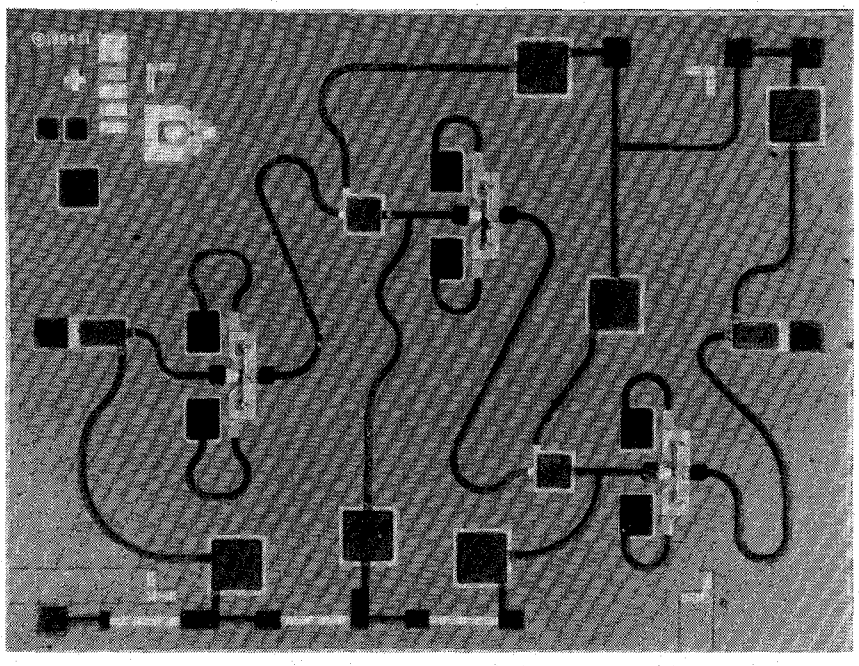

Fig. 8. Monolithic three-stage LNA.

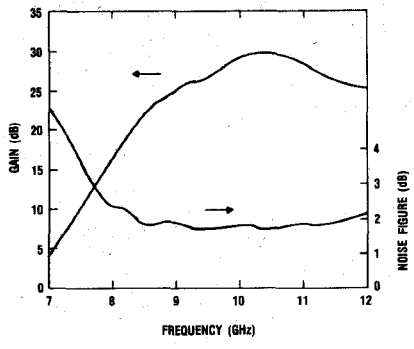

Fig. 9. LNA gain and noise figure performance.

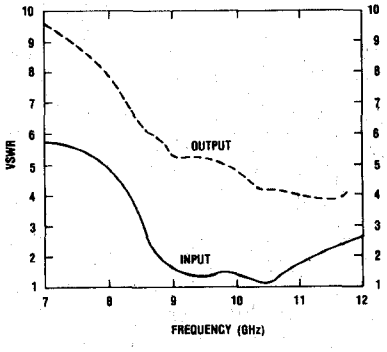

Fig. 10. LNA VSWR performance.

TABLE III
SLICE SUMMARY OF LNA MEASUREMENTS AT 10 GHZ

SLICE #	# LNAs TESTED	NF (dB)			GAIN (dB)			INPUT VSWR		
		LO	HI	AVG.	LO	HI	AVG.	LO	HI	AVG.
1	10	1.9	2.2	2.0	28.2	32.4	30.0	1.1	1.4	1.2
2	4	1.8	2.0	1.9	29.5	32.0	30.9	1.2	1.4	1.3
3	4	1.9	2.0	1.9	28.3	32.1	30.4	1.1	1.4	1.2
4	4	1.9	2.2	2.0	26.5	31.6	28.7	1.1	1.2	1.2
5	2	2.3	2.4	2.3	27.2	27.6	27.4	1.3	1.3	1.3
6	4	2.0	2.1	2.1	28.7	30.8	30.0	1.1	1.3	1.2
7	5	2.1	2.4	2.2	25.1	29.3	26.9	1.1	1.4	1.2
8	1	2.2	2.2	2.2	30.0	30.0	30.0	1.4	1.4	1.4
9	1	2.0	2.0	2.0	30.1	30.1	30.1	1.4	1.4	1.4
TOTAL	35	1.8	2.4	2.0	25.1	32.4	29.4	1.1	1.4	1.2

from nine slices highlight the advantages of a series feedback design to achieve very repeatable performance.

ACKNOWLEDGMENT

The authors wish to thank R. E. Williams for processing support and S. F. Goodman and J. Wright for technical assistance.

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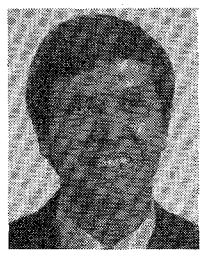

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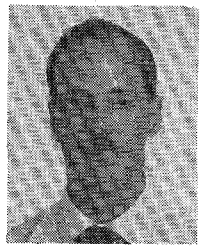

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